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Identification card.

Abstract:

An IC card includes a processor (1), a first memory (11) for storing therein a system program which runs on the processor (1) and which is associated with a basic operation of the IC card, a second memory (9) for storing therein an application program which runs on the processor (1) and which corresponds to a usage of the IC card, a third memory (8) for storing therein data processed by the processor (1), an input/output unit (2) for effecting input and output operations of programs and data, a program stop section (6) for stopping the program being executed on the processor (1) at a specified address; and a data output section (4) for supplying the input/output unit (2) with either one of a content of a register in the processor (1) and a content of an area at an address of at least one of the first, second, and third memories (11, 9, 8) when the program running on the processor (1) is stopped.

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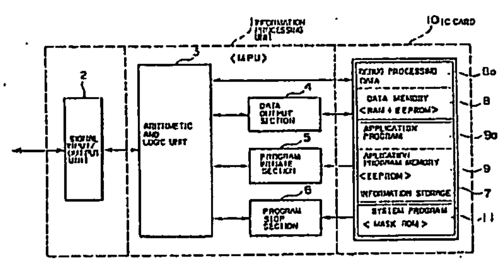
(54) **Identification card.**

(57) An IC card includes a processor (1), a first memory (11) for storing therein a system program which runs on the processor (1) and which is associated with a basic operation of the IC card, a second memory (9) for storing therein an application program which runs on the processor (1) and which corresponds to a usage of the IC card, a third memory (8) for storing therein data processed by the processor (1), an input/output unit (2) for effecting input and output operations of programs and data, a program stop section (6) for stopping the program being executed on the processor (1) at a specified address; and a data output section (4) for supplying the input/output unit (2) with either one of a content of a register in the processor (1) and a content of an area at an address of at least one of the first, second, and third memories (11, 9, 8) when the program running on the processor (1) is stopped.



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Description

IDENTIFICATION CARD

BACKGROUND OF THE INVENTION

The present invention relates to an Integrated Circuit (IC) card, and in particular, to an IC card in which an operation program loaded therein can be easily debugged.

IC cards are employed as cards of various financial facilities and those of identification of workers or employers. Moreover, the IC cards have been increasinly used as cash cards of banks, credit cards for various transactions, and cards for purchasing tickets and the like of traffic facilities.

These cards have been put to use in various areas of applications. IC cards issued in association with various transactions have content of data to be processed depending on the respective transactions, and processing manners of the data vary among the cards. For these reasons, the processing programs of such cards are, prepared to correspond to terminals or host computers (the host computers and terminals are representatively referred to as terminals herebelow) on which the processing programs are to be respectively executed. The processing program includes a control program (to be referred to as a basic processing program) for controlling basic operations such as data read/write operations and communications; furthermore, a processing program (to be referred to as an application program in this specification) for assigning particular functions depending on specifications of the IC card after the card is manufactured. In this situation, an IC card, of a so-called down-load processing type has been proposed to be put to practice in which in association with terminals corresponding to the various transactions, the application programs are respectively written later therein. In the IC card of the down-load processing type, an application program corresponding to the specification of the IC card is written after the manufacturing thereof. In this operation, the application program to be loaded into the IC card is ordinarily developed by use of a personal computer or the like in many cases.

The application program created depending on a purpose and processing functions of the IC card is required to be debugged through an operation test as the IC card for a confirmation of the operation. When the operation test and debugging are achieved on the developed application program, an operation test program and a debug program necessary therefor are usually loaded on the side of the personal computer. The operation test is interactively conducted according to the programs in such manner that data is externally supplied to the IC card loaded with the prepared application program so as to check the response to the supplied data.

The interactive operation above is achieved in association with the respective function items of the IC card in such manner that on receiving response data from the IC card, the personal computer or the like judges the content of the test and that the debugging of the application program is accomplished by executing the application program loaded in the personal computer. In consequence, the debugging of the application program in the card requires a large number of operation steps and hence the program development efficiency is lowered. Moreover, in the program development, developing tools are necessary in correspondence with the application program to be the development object, which complicate the configuration of the development system and which make the program development cost soar.

In addition, since appropriate data is to be supplied to the personal computer in order to achieve the operation test and the program debugging, the content of the basic processing program loaded in the IC card is required to be known. Consequently, when the program is developed by an external program firm other than the basic processing program developer, information of the content of the basic processing program in the IC card is required to be supplied to the external program firm. This leads to a disadvantage that the security of the basic control program cannot be preserved.

SUMMARY OF THE INVENTION

It is therefore an object of the present invention to provide an IC card having a high development efficiency for developing an application program to be loaded in the IC card, thereby solving the problems above.

Another object of the present invention is to provide an IC card facilitating an operation test and a debugging of an application program to be executed in the IC card.

Still another object of the present invention is to provide an IC card improved for developing an application program to run in the IC card by a small-scale development system not having a debug function.

Another object of the present invention is to provide an IC card in which only a portion of an application program down-loaded in the IC card is executed to supply a result of the execution to a terminal connected to the IC card, thereby evaluating the portion of the application program.

In order to achieve the objects above, the IC card according to the present invention includes a processor, a first nonvolatile memory section storing therein a basic processing program which runs on the processor to conduct a communication and a memory control, a second nonvolatile memory section which is a rewritable memory for storing therein through a down-load operation an application program to be written depending on a purpose of the card after the card is manufactured, a third memory section comprising a rewritable nonvolatile or volatile memory for storing therein various processing data items, program initiate processing

means for causing the processor to execute an application program (communicating data between the card and an external device) beginning from an execution start address set in the second nonvolatile memory section, program stop processing means for stopping an execution of the application program when a stop condition set during the execution of the application program is satisfied, and data output processing means for outputting to an external device a content at least one selected from registers in the processor, other registers, an area indicated by a specified address of the second nonvolatile memory unit, and an area indicated by a specified address of the third memory unit such that at least one of the execution start address and the stop condition and data output is set by use of an external device.

As described above, since the IC card is provided with program initiate processing means for executing from an arbitrary address an application program loaded from an external device into the IC card, program stop processing means for stopping the application program during an execution thereof when an arbitrary stop condition such as one associated with a stop address is satisfied, and data output processing means for effecting processing to output information from the memory units, the registers, and the like of the IC card to an external device; after a developed application program is stored in the IC card, the application program can be partially executed so as to output a result of the execution to the external device.

As a result, the operation test of the IC card and the debugging of the developed application program are facilitated. The operation of the developed program to be the development object is identical to the operation to be conducted in the actual operation environment. In consequence, the IC card is suitable for the development of the application program thereof in a small-scale developing system not having a debug function.

BRIEF DESCRIPTION OF THE DRAWINGS

These and other objects and advantages of the present invention will become apparent by reference to the following description and accompanying drawings wherein:

FIG. 1 is a block diagram schematically showing an embodiment to which an IC card is applied according to the present invention;

FIG. 2 is a schematic block diagram of an alternative embodiment of an IC card according to the present invention;

FIG. 3 is an explanatory diagram useful to explain transition of the operation state of the IC card;

FIG. 4 is a schematic diagram showing a format of a mode switch command;

FIG. 5 is a diagram showing a mode switch sequence; and

FIGS. 6 and 7 are diagrams showing respective configurations of the program stop processing section.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

The configuration of FIG. 1 includes an IC card 10 which is installed in IC card reader/writer or the like to communicate data with it and numeral 1 indicates an information processing section 1 (comprising a microprocessor, MPU). The system further includes a signal input/output unit 2 of the IC card 10. The MPU 1 communicates data with the terminal via the signal input/output unit 2.

When manufacturing an IC card, the system program or the basic processing program is desirably stored in a mask read-only memory (ROM). When the IC card is issued, information items such as a secret code or a password of a card user and areas to be set in the memory depending on a purpose of the IC card are down-loaded or stored in the ROM together with the application program developed created depending on the utilization purpose. The information items may further include a key of the issuer, an account number of a banking card of the user, and attribute information items such as a name and an address of the card user. The application program thus stored in the ROM is subjected to an operation test through an actual usage of the IC card, thereby achieving the debugging.

In an ordinary operation of the IC card 10 after the issuance thereof, the MPU 1 executes a predetermined processing in accordance with an application program 9a stored in the operation program memory section 9. In a random access memory (RAM) area of a data memory section 8 comprising an RAM and an electrically erasable programmable ROM (EEPROM), data transferred from the terminal, read data, resultant data, and the like are temporarily stored. These data items are transferred between the IC card and the terminal having the IC card reader/writer or the like. Incidentally, the EEPROM region of the data memory section 8 is ordinarily loaded with registration data such as history information of shopping and banking transactions conducted by use of the IC card.

The operation program of the IC card 10 is transferred through a down loading from the terminal so as to be stored as the application program 9a in the operation program memory section 9 comprising an EEPROM or the like in the information storage or memory 7. As a result, the IC card 10 is provided with the functions such that the MPU 1 operates according to the program and that the IC card 10 executes processing in association with the purposes and specifications thereof.

The MPU 1 has functional blocks including an arithmetic and logic unit 3, a data output section 4, a program initiation processing section 5, and a program stop processing section 6. Incidentally, a portion of or all of these constituent elements may be implemented as hardware in a form of a circuit or may be realized by executing by means of the MPU 1 the basic processing program associated therewith and stored in a system program memory unit 11 or the like comprising a mask ROM in the information storage 7 (or in the MPU 1). Furthermore, these functional blocks may be materialized by use of a

combination of hardware and software.

Under the conditions above, the arithmetic and logic unit 3 selectively executes several basic programs stored in the system program memory section 11 and the application program 9a so as to achieve various processing specified. The basic processing programs include a program write program to write data (application program) supplied from an external device for the application program 9a in an area of the operation program memory section 9, a debug processing data write program or debugger program to load in a debug processing data area 8a of the data memory 8 with debug processing data including information to specify an initiating position or an execution start address of the application program 9a and/or an initating condition, information specifying a register or the like associated with read data, and information specifying a stop position or a stop address of the application program 9a and/or a stop condition; supplied from an external device and a mode switch program to change over the IC card 10 between an ordinary operation mode and a development mode. These programs are stored in the system program memory 11.

Referring to FIGS. 4 and 5, a description will be given of a method of changing over the mode. As shown in FIG. 5, the system program 11 includes a basic processing program, a debugger program, and a mode switch program. Communications with an external device are conducted by the basic processing program. On receiving a mode switch command via the signal input/output unit 2, the basic processing program orders to store the received command in the RAM region of the data memory 8 and then jump to the mode switch program. The command includes a data block 102 in which a mode identifying information item of a switch objective mode (the ordinary or development mode) is set. The mode switch program order to store the mode identifying information in the EEPROM region of the data memory 8. In a case where the EEPROM is used for this purpose, even when the power is turned off, the previous state is preserved, which is effective in a program developing phase. In contrast, the mode identifying information may be stored in the RAM region of the data memory 8. In this case, when the power is turned off, the mode information item is initialized by the reset operation. When the content of the specified mode identifying information indicates the development mode, the mode switch program initiates the debugger program (FIG. 5) stored in the system program memory 11. The debugger program sets to the data memory 8 address information items and the like to be respectively used in the data output section 4, the program initiate section 5, and the program stop section 6 and then initiates these sections. When these components are implemented by hardware units, the initiate operations are achieved by generating operation enable signals for the respective units. If these components are softwarewise realized, the system achieves initialization of the components.

Each of the programs above is selected for initiation when the MPU 1 decodes a command supplied from the external device so as to be executed by the arithmetic and logic unit 3. When the mode switch program is here selected to be executed, as indicated by an arrow 33 of FIG. 3, the operation of the IC card 10 is changed over from the ordinary operation mode 31 to the development operation mode 32 or vice versa. When the IC card 10 is set to the development mode, the data output section 4, the program initiate section 5, and the program stop section 6 of FIG. 1 are respectively initiated to the operative state. On the other hand, in the ordinary operation mode, these sections 4-6 are in the stopped state, and the arithmetic and logic unit 3 sets up the basic processing program and the application program 9a to the executable state. Incidentally, when a mode changeover is to be achieved in response to a signal from an external device, as already described in conjunction with FIG. 4, the mode switch program is started by use of a command code with mode identifying information loaded in the data block 103.

In the ordinary processing mode, when the command from the external device is a write command of the application program 9a, a so-called down loading is achieved in response thereto so as to execute the program write program to store the data of the application program 9a in the operation program memory 9. If the command indicates a write command of the debug processing data, the debug processing data write program loades the debug processing data storage area 8a of the data memory 8 with the debug processing data sent from the external device.

Incidentally, the application program 9a is to be developed, when the IC card 10 is issued, depending on a utilization purpose thereof. In the development of the program 9a, a personal computer or the like is used to generate the program 9a. At the issuance of the IC card 10, the program 9a is written in the IC card 10 according to the program write program and then the operation of the program is confirmed. In the initial stage of the development, since the prepared application program usually includes wrong portions, the program is required to be debugged. On the other hand, the basic processing program stored in the system program memory 11 is generally written as a basic control program or a system program in the IC card when the card is manufactured.

Assume here that the IC card 10 has already been loaded with the various basic processing programs in the system program memory 11, that the data output section 4, the program initiate section 5, and the program stop section 6 are ready to start and to stop the application program 9a at an arbitrary address according to the debug processing data, and that the debug processing data is freely set from the external device. In consequence, the operation test and the debug of the application program 9a are executable in a state associated with the actual operation of the IC card 10 corresponding to specified portions of the program 9a. Next, a procedure of the debug will be described.

First, an application program under development

is down-loaded by the program write program initiated in response to a command supplied from an external device such as a terminal, thereby writing the program 9a in the operation program memory 9 of the IC card 10. Thereafter, the debug processing data write program is initiated by use of a command from the external device so as to write the debug processing data in the debug processing data storage area 8a of the data memory 8. The mode switch program is then started by use of the external device to change over the IC card 10 from the ordinary operation mode to the development mode.

As a result of the mode change-over operation, the data output section 4, the program initiate section 5, and the program stop section 6 are respectively initiated. The program initiate section 6 references a start address stored in the debug processing data storage area 8a to instruct the arithmetic and logic unit 3 to start excution from a start address specified in a jump instruction supplied from the external device, thereby initiating the application program 9a from the start address.

On the other hand, the program stop section 6 starts its operation after the application program 9a is initiated to monitor stop information stored in the debug processing data storage area 8a and address data, control data, and other data transmitted onto a bus of the MPU 1. On sensing a matching condition of a stop condition, the program stop section 6 causes the arithmetic and logic unit 3 to interrupt the application program 9a being executed.

Referring now to FIGS. 6 and 7, a description will be given of a method of interrupting the program execution. FIGS. 6 and 7 show examples in which the program stop section 6 is implemented by use of hardware and software, respectively. In the program stop unit 6 of FIG. 6, a stop address set by the debugger program is stored in a stop register 62, and a comparator 63 is connected to an address bus 31 to compare memory address information processed by the arithmetic and logic unit 3 with a value of the stop register 62. In addition, the comparator 63 is initialized by the debugger program such that an operation enable signal 65 is supplied to the comparator 63, which is accordingly set to the operable state. When the application program 9a is started and an address on the address bus 31 is identical to the address set to the stop register 62, an interruption signal 64 is generated to interrupt the processing of the application program 9a so as to pass control to the program stop section 6 indicated by the interruption processing vector. In this manner, the operation of the application program 9a may be stopped by use of the program stop section 6 implemented by the hardware. Next, a description will be given of an example in which the program stop section 6 is materialized by use of software. The program stop section 6 temporarily saves a program code (for example, 96H) of a stop address set at the initialization so as to the reafter replace the stop address program code with a code (for example, OOH) which can be executed by the arithmetic and logic unit 3. After the application program 9a is initiated by the program initiate section 5, when an attempt is made to execute the program code at the stop address in the application program 9a, a trap error occurs (because an attempt is made to execute an unexecutable program code). As a result of the trap error, an internal interruption takes place, which causes control to jump to an address stored in the trap interruption vector as indicated with an arrow 77. The address stored in the trap interruption vector is beforehand set to the first address of the program stop section 6 or an address where the processing is to be executed after the stopage of the application program 9a. After the application program 9a is interrupted, when the program stop section 6 starts its operation, the stop address program code saved in advance is restored (to 96H). In this manner, the execution of the application program 9a can be stopped.

The data output section 4 traces, depending on specifying information such as a register associated with read data, information items or the like stored in a specified internal memory, a register, and at a specified address of the information memory 7 or changes of the information items so as to sequentially store the trace data or data in the internal memory and the register in the predetermined storage areas of the data memory 8. When the execution of the application program 9a is stopped, the data output section 4 causes the arithmetic and logic unit 3 to read from the data memory unit 8 information items stored in the specified internal memory, the register, and at the specified address of the information storage 7 or trace information associated with the address. The data output unit 4 conducts a control to transmit the information as response information from the IC card 10 to the external device via the arithmetic logic unit 3 and the signal input/output unit 2.

Incidentally, output timing of the trace information thus attained from the data output section 4 and the contents of the area at the address, the internal memory, and the register may be selected as follows. Namely, in place of achiving the output operations when the execution of the application program 9a is stopped, the execution control of the application program 9a may be temporarily stopped at a predetermined timing specified so as to supply, by use of an interruption processing, to the arithmetic and logic unit 3 with the contents of the specified address, the specified internal memory, and the specified register. In this case, the data output section 4 need not necessarily conduct the processing to store output data in the data memory unit 8.

With the configuration above, when a memory address as a read object is supplied from an external device in advance, the data output section 4 reads the content of the data memory 8 or the operation program memory 9. The obtained data content is transmitted via the arithmetic and logic section 3 and the signal input/output unit 2 to the external device. In addition, the conditions associated with the application program 9a in a range from the start of the program 9a to the termination thereof can be arbitrarily set and modified in association with the test or debug locations from the external device.

FIG. 2 shows an IC card in which in association

with the configuration of the MPU 1, the operations of the data output section 4 and the program initiate section 5 are implemented by a program stored in the operation program memory 9 and the operation of the program stop section 6 is realized by a hardware constitution of a stop condition detector circuit 61 including a program, a comparator, and a register. The programs of the data output section 4, the program initiate section 5, and the program stop section 6 are stored as a development operation program 92 in the operation program memory 9. The application program 9a as a development object is similarly stored as an ordinary operation program 91 in a predetermined region of the operation program memory 9.

These two kinds of operation programs operate in two states, namely, in a development operation mode (associated with the development mode above 9) and an ordinary operation mode. The ordinary operation mode is a state in which the ordinary operation program 91 operates in an environment identical to the actual operation environment. In the development operation mode, the ordinary operation program 91 is controlled by the development operation program 92 such that the initiation and the termination of the ordinary operation program 91 are achieved at an arbitrary address established and that a stop condition can be set from an external device via the development operation program 92.

That is, the development operation program 92 of this example is prepared as a processing program of which various functions such as an execution of the ordinary operation program 91, a termination thereof, an output of the internal state of the program 91, a setting of internal data thereof, and a forcible termination of the program execution can be specified by supplying particular information items from the external device. The function to set internal information is disposed to arbitrarily set the memory and register contents in the IC card 10 from the external device. The forcible termination function is adopted to forcibly terminate the ordinary operation program 91 when the execution thereof cannot be stopped in an ordinary manner due to an occurrence of a state disabling the program execution control. A signal to finish the execution in this case is supplied from the external device via the signal input/output unit 2 to the arithmetic and logic unit 3. Under the conditions above, owing to the provisions of these functions, the execution and termination of the ordinary operation program 91, the output of the internal state of the program 91, and the setting of the internal information items thereof are repeatedly carried out so as to efficiently achieve the development, the operation test, and the debugging of the application program.

Particularly, a runaway often occurs in a program under development. In consequence, by inputting a forcible termination signal from the signal input/output unit 2 to interrupt the program operation at a runaway or the like thereof, the program development may be effectively conducted.

Switching between the ordinary operation mode and the development operation mode is automatically accomplished without using the mode switch program, as shown in FIG. 3, by initiating the ordinary operation program 91. That is, when an execution of the ordinary operation program 91 is stopped or when the program 91 is not initiated, the system automatically changes over to the development operation mode. For this purpose, mode identifying information is stored in the RAM area of the data memory 8, and when the system is powered, the state immediately preceding the reset operation is set as the development operation mode. In consequence, the IC card 10 may change over to the state in which the development operation program 92 is initiated.

With the provisions above, during an operation of the ordinary operation program 91, the test can be achieved under an actual operating environment. Incidentally, the mode switch operation may be conversely executed such that when the development operation program 91 is initiated, the development operation mode is automatically set.

As described above, although the embodiments above include the system program memory 11 in addition to the MPU 1, the memory 11 may be disposed in the MPU 1. Furthermore, the information memory 7 is arranged outside the MPU 1; however, the memory 7 may also be located in the MPU 1. The configurational relationships between the blocks of the information memory 7, the signal input/output unit 2, and the MPU 1 of the embodiments above have been described only by way of example and hence the present invention is not restricted by the embodiments.

Furthermore, the internal constitution of the information memory 7 is not restricted by the configurations of the embodiments. Namely, the constitution may comprise an appropriate combination of various memories including an EEPROM, an RAM, and an ROM. In this case, a memory element may be subdivided into subareas for the control thereof. In addition, as the volatile memory, an RAM as well as a volatile EEPROM may be employed.

While particular embodiments of the invnetion have been shown and described, it will be obvious to those skilled in the art that various change and modifications may be made without departing from the present invention in its broader aspects.

Claims

1. An IC card comprising:

a processor (1);

a first memory (11) for storing therein a system program which runs on said processor (1) and which is associated with a basic operation of said IC card;

a second memory (9) for storing therein an application program which runs on said processor (1) and which corresponds to a usage of said IC card;

a third memory (8) for storing therein data processed by said processor (1);

an input/output unit (2) for effecting input and output operations of programs and data;

program stop means (6) for stopping the program being executed on said processor (1) at a specified address; and
data output means (4) for supplying said input/output unit (2) with either one of a content of a register in said processor (1) and a content of an area at an address of at least one of said first, second, and third memories (11, 9, 8) when the program running on said processor (1) is stopped.

2. An IC card according to Claim 1 further including means (11, 6) operative in response to mode identifying information included in a mode switch command inputted via said input/output unit (2) of said IC card in order to control an execution of the application program to be executed in an ordinary operation mode (31) for causing said program stop means (6) to operate to stop the program on said processor (1).

3. An IC card according to Claim 1 wherein said program stop means (6) includes a register (62) for keeping therein a stop address to be compared with an address signal received from an address bus connected to said processor (1).

4. An IC card according to Claim 1 wherein said program stop means (6) includes means for saving a content of an address for a stoppage in the application program and for keeping in place thereof a command code which can be executed by said processor (1).

5. An IC card comprising:
a processor (3);
a first nonvolatile memory section (11) for storing therein a basic processing program of said processor (3);
a rewritable second nonvolatile memory section (9) for storing therein an application program associated with the basic processing program;
a third memory section (8) comprising a rewritable nonvolatile or volatile memory for storing therein various kinds of processing data, thereby achieving data communications with an external device,
said IC card further including:
program initiate processing means (5) for causing said processor (3) to execute the application program beginning from an execution start address set to said second nonvolatile memory section (9);
program stop means (6) operative during an execution of the application program for stopping the execution when a specified stop condition to stop the execution is satisfied; and
data output means (4) for supplying the external device with a content of either one of an internal register of said processor (3), another register, and at least one selected from areas indicated by addresses specified in said second nonvolatile memory section (9) and in said third memory section (8),
at least either one of the execution start address and the stop condition is set by use of the external device.

6. An IC card according to Claim 5 having an ordinary operation mode (31) and a development mode (32),
said ordinary operation mode (31) being disposed to enable said IC card to operate as an ordinary IC card and to enable the application program to be executed;
said development mode (32) being disposed to enable an execution of the application program to be controlled through operations of said program initiate processing means (5), said program stop processing means (6), and said data output processing means (4),
either one of said ordinary operation mode (31) and said development mode (32) being selected by the external device.

7. An IC card according to Claim 5 wherein said first nonvolatile memory section (11) comprises a mask ROM.

8. An IC card according to Claim 5 wherein said second nonvolatile memory section (9) and said third memory section (8) comprise an EEPROM.

9. An IC card according to Claim 8 wherein said second nonvolatile memory section (9) and said third memory section (8) are integrated in an EEPROM.

10. An IC card according to Claim 6 wherein said program initiate processing means (5) and said data output processing means (4) are included in said processor (3).

11. An IC card according to Claim 6 wherein said first nonvolatile memory section (11) contains a mode switch program effecting a change-over operation between said ordinary operation mode (31) and said development mode (32).

12. An IC card according to Claim 11 wherein said first nonvolatile memory section (11) comprises a mask ROM.

13. An IC card according to Claim 6 further including a debug data storage area to be loaded with debug data.

FIG. 1

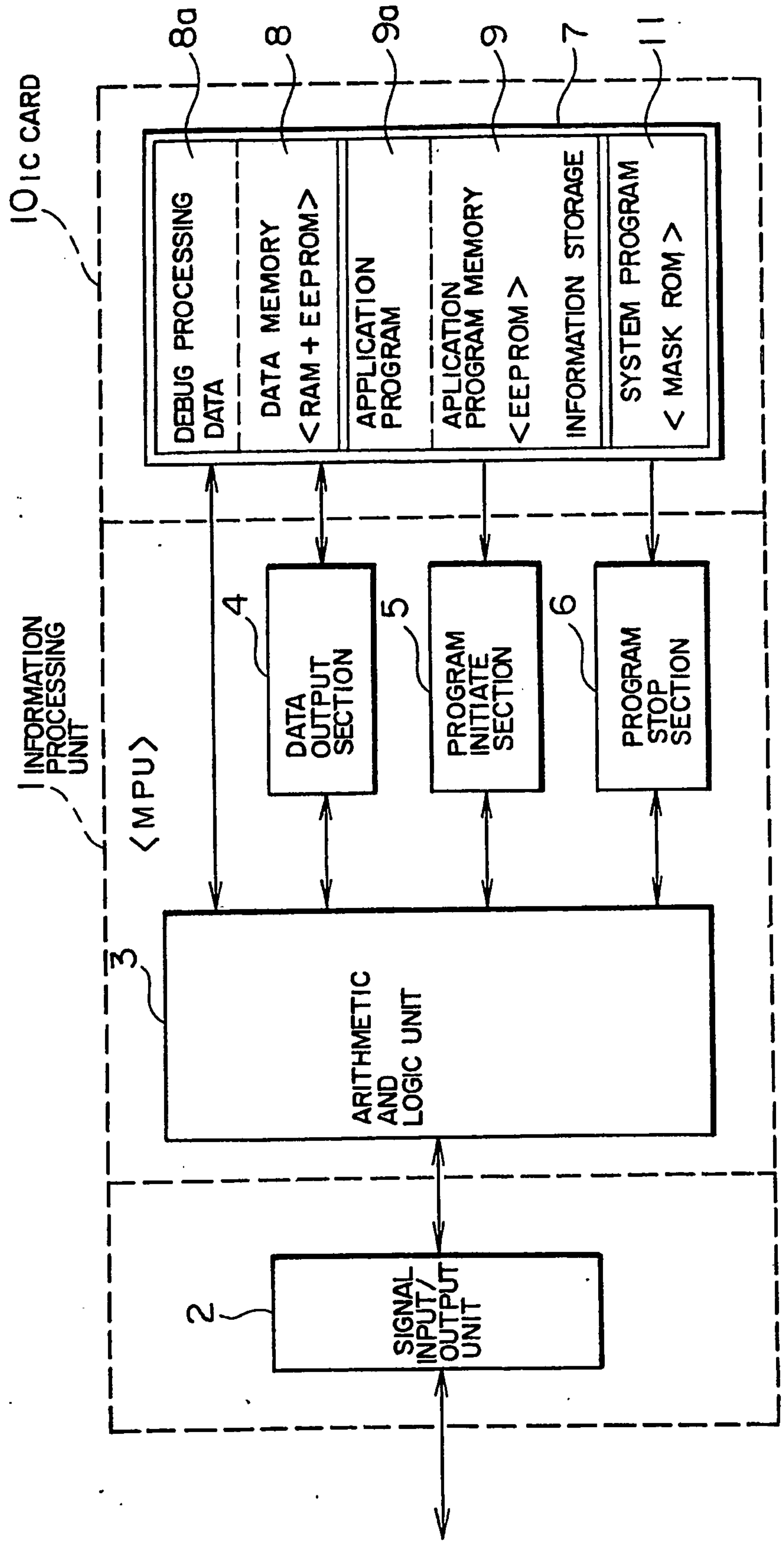
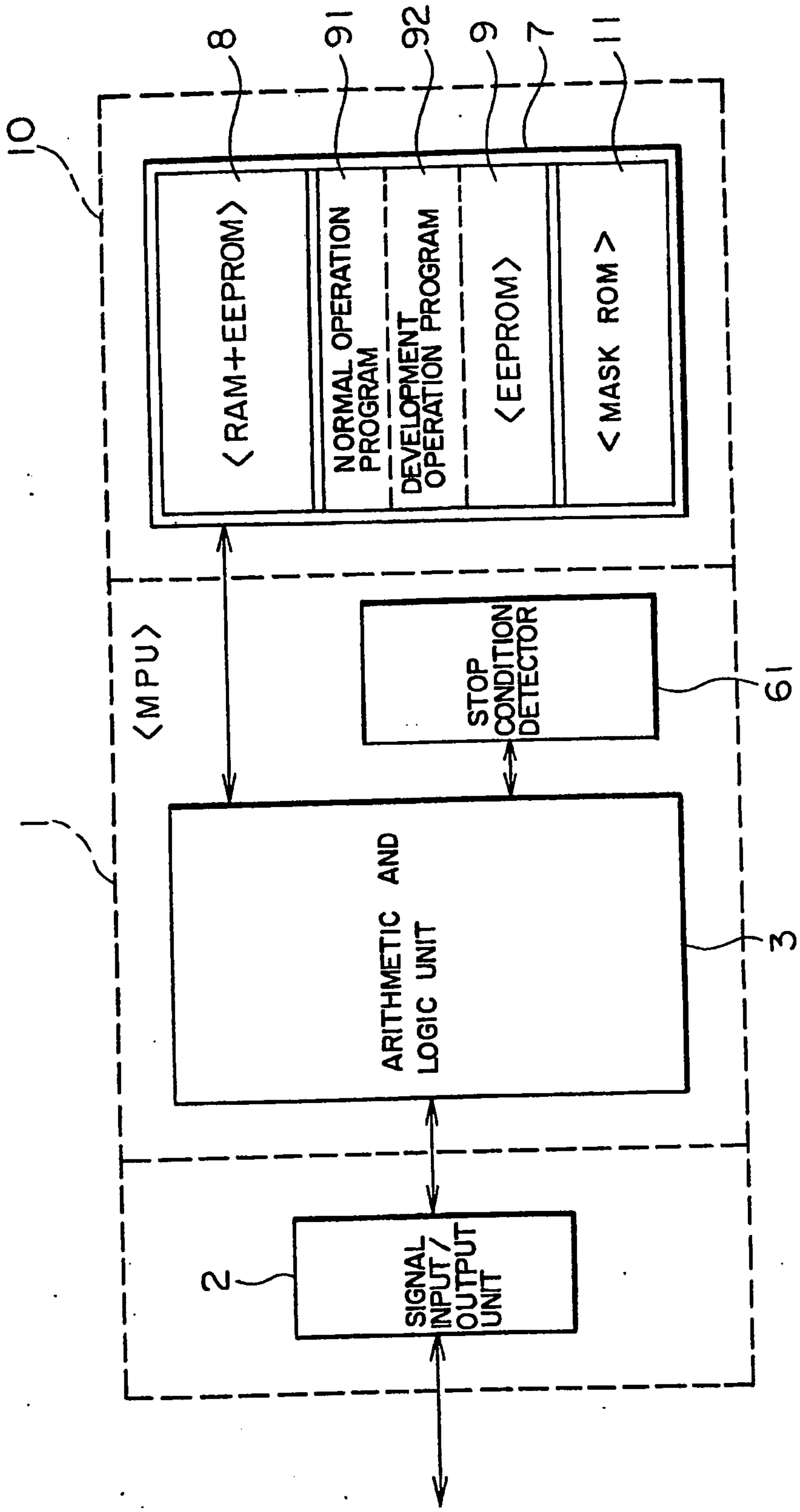

10 IC CARD
DEBUG PROCESSING DATA
DATA MEMORY
<RAM + EEPROM>
APPLICATION PROGRAM
APLICATION PROGRAM MEMORY
<EEPROM>
INFORMATION STORAGE
SYSTEM PROGRAM
< MASK ROM >
8a
8
9a
9
7
11
1 INFORMATION PROCESSING UNIT
〈MPU〉
DATA OUTPUT SECTION
PROGRAM INITIATE SECTION
PROGRAM STOP SECTION
4
5
6
3
ARITHMETIC AND LOGIC UNIT
2
SIGNAL INPUT/ OUTPUT UNIT

FIG. 2



10
8
91
92
9
7
11
<RAM+EEPROM>
NORMAL OPERATION PROGRAM
DEVELOPMENT OPERATION PROGRAM
<EEPROM>
<MASK ROM>
<MPU>
STOP CONDITION DETECTOR
61
1
ARITHMETIC AND LOGIC UNIT
3
2
SIGNAL INPUT/OUTPUT UNIT

FIG. 3

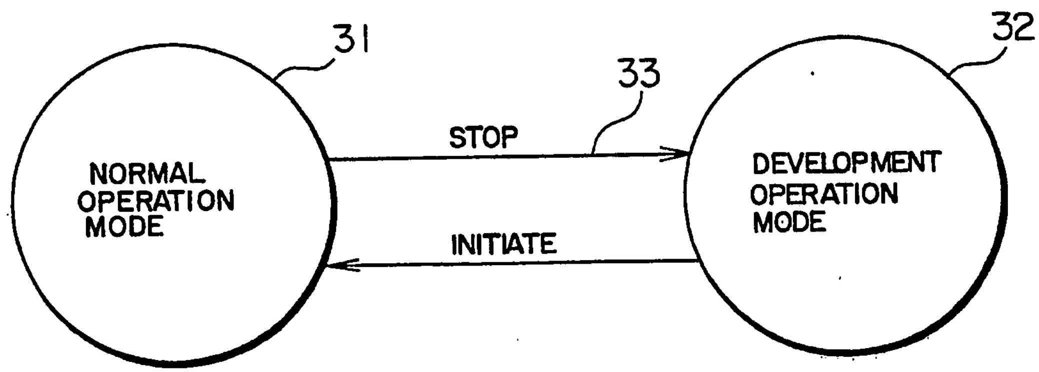

31
32
33
NORMAL OPERATION MODE
DEVELOPMENT OPERATION MODE
STOP
INITIATE

FIG. 4

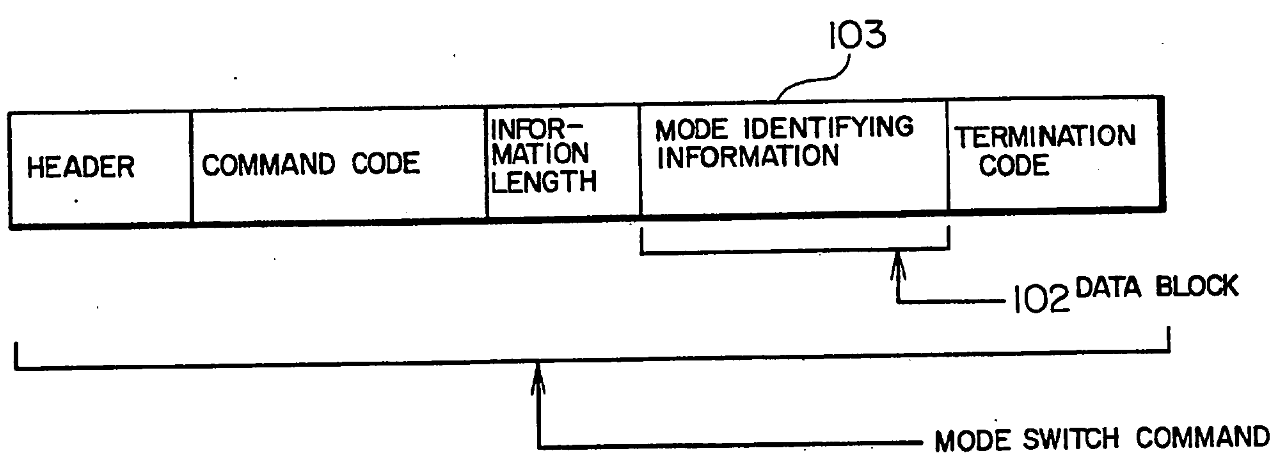

103
HEADER
COMMAND CODE
INFOR-MATION LENGTH
MODE IDENTIFYING INFORMATION
TERMINATION CODE
102 DATA BLOCK
MODE SWITCH COMMAND

FIG. 5

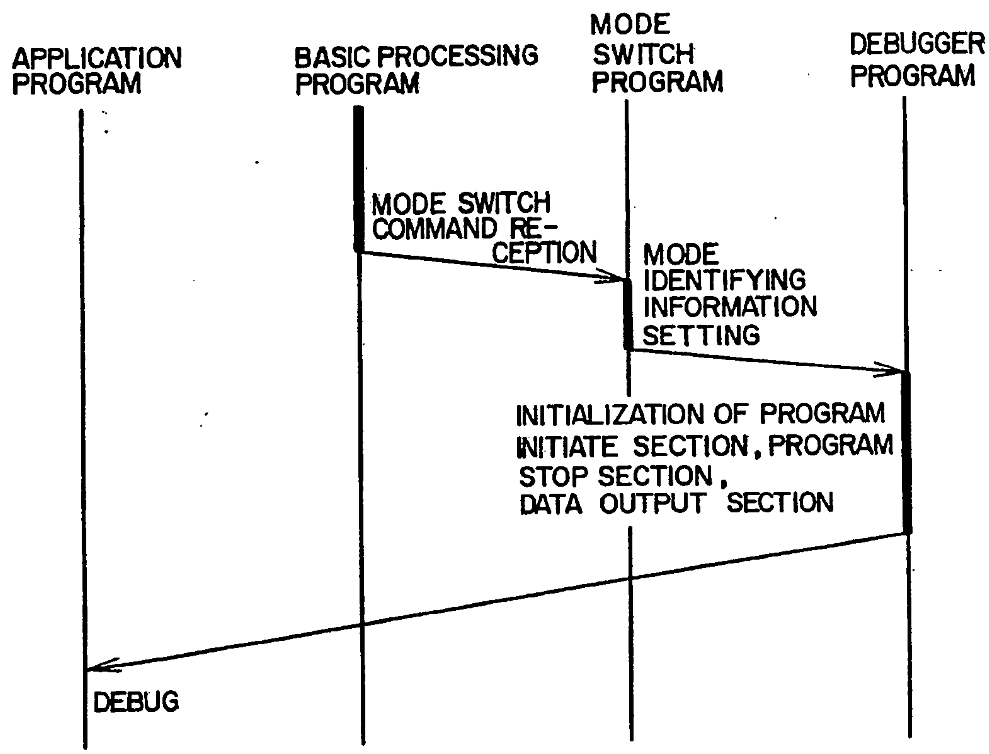

APPLICATION PROGRAM
BASIC PROCESSING PROGRAM
MODE SWITCH PROGRAM
DEBUGGER PROGRAM
MODE SWITCH COMMAND RE- CEPTION
MODE IDENTIFYING INFORMATION SETTING
INITIALIZATION OF PROGRAM INITIATE SECTION, PROGRAM STOP SECTION, DATA OUTPUT SECTION
DEBUG

FIG. 6

PROGRAM STOP SECTION 6
IMPLEMENTED BY HARDWARE

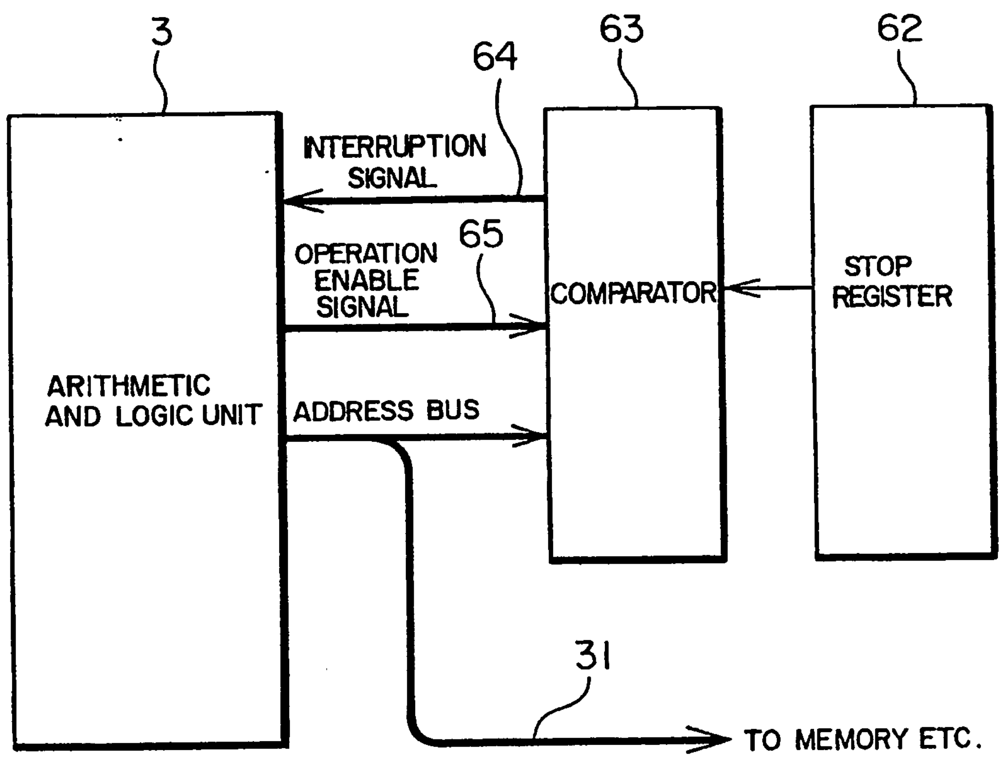


FIG. 7

PROGRAM STOP SECTION
IMPLEMENTED BY SOFTWARE